MIPS Embedded Software Solutions

MIPS Development Tools

Green Hills Software provides a comprehensive set of development tools for MIPS-based™ applications:

Optimizing Compilers

- C
- C++/Embedded C++
- FORTRAN
- Ada 95

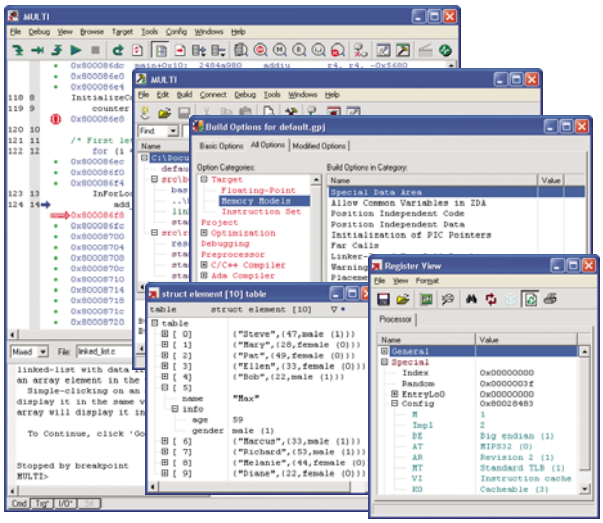
MULTI® Integrated Development Environment

- Source Level Debugger
- Project Builder
- Language-Sensitive Text Editor
- Version Control System
- Graphical Browser
- Performance Profiler
- Run-Time Error Checking
- Code Coverage Analysis
- RTOS EventAnalyzer
- Remote Target Connection
- Instruction Set Simulators

Real-Time Operating System Support

- *velOSity*™ royalty-free microkernel
- INTEGRITY® royalty-free RTOS
- Express Logic's ThreadX® RTOS

For general information about each of these product offerings, please refer to our "Total Solutions for Embedded Software Development" brochure. The following are aspects of these products specific to the MIPS architecture.



MULTI provides an exhaustive set of project build and debug features for MIPS processors, designed to reduce the time developers spend organizing projects and finding and fixing bugs.

Processors Supported

MIPS32™	R4000®	RC500
MIPS64™	R41xx	TX19xx
MIPS32 4K™ family	R4200®	TX49
MIPS32 4KE™ family	R43xx	TX390x
MIPS32 4KS™ family	R4400®	TR410x
MIPS32 M4K	R4500	VR43xx
MIPS64 5K™ family	R4600	VR50xx
MIPS64 20K™ family	R5000®	VR41xx
MIPS64 25K family	RC30xx	VR54xx
CW40xx	RC323xx	VR5500
R3000®	RC4700	
R37xx	RC46xx	

MIPS Optimizing Compilers

The Green Hills Software's MIPS optimizing compilers use a common code generator with architecture and processor specific optimizations. MIPS-specific features include:

- **Processor Options**—Specific to each MIPS architecture and processor supported for optimal performance. This setting determines the instructions permitted as well as the pipeline optimization strategy used.
- **Position Independent Code (PIC) and Data (PID)**—Allows code and data to be placed anywhere in memory and still run correctly.
- **MIPS16e™ Instruction Set**—Generates code for the MIPS16e ASE.
- **MIPS-3D™**—Supports the MIPS-3D ASE through intrinsic functions.
- **64-bit Integers**—Supports 64-bit data types, constants, and expressions for all MIPS processors.
- **Far Function Calls**—Handles code that exceeds the limits of the MIPS call instruction.
- **Inline Prologue**—Generates inlined code or calls a routine when saving and restoring registers.
- **Linker Optimizations**—The Green Hills Linker optionally performs additional optimizations for speed and size.
- **MIPS32/MIPS64 Release 2**—Generates code for the latest version of the MIPS architecture.
- **Memory Allocation Functionality—**The alloca() function provides a mechanism to allocate a fixed size of memory that is automatically freed when the current function exits.

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- **Small Data Area**—The Green Hills Compilers collect frequently accessed variables into a 64KB block of memory. This enables single instruction access to data within this block, saving code size and improving performance.

Compliance with Industry Standards

Green Hills C/C++ Compilers fully conform to ANSI/ISO industry standards, and include optional enforcement of MISRA C programming guidelines.

Run-Time Libraries

A complete implementation of the C, C++, EC++, Ada 95 and FORTRAN libraries are included in compiler distributions. Full featured start-up code and libraries include automatic copy of data from ROM to RAM and system call emulation.

MIPS16e™ and MIPS16™

Green Hills C/C++ Optimizing Compilers provide user-selectable optimization options that trade-off code size vs. execution efficiency. In particular, for the MIPS16e and MIPS16 ASEs, benchmark tests have proven the effectiveness of the Green Hills Compilers in producing the smallest executable file from a given source base.

CodeBalance

Green Hills Software offers CodeBalance®, a powerful utility program that analyzes performance profiling data, enabling the user to make critical execution speed/code size trade-offs. Other compilers must compile all functions in a file either in 16 or 32-bit mode. CodeBalance achieves greater code-size reduction with minimal increase in execution time by performing function-specific 16-bit mode compilation. Green Hills Software offers additional optimizations on a function-by-function basis with the powerful #pragma-based capability.

The MULTI Integrated Development Environment

MULTI provides a host-based (Windows, Solaris, HP-UX and Linux) graphical environment for MIPS target development. Host-target connectivity is provided through a variety of means, depending on the target environment. MULTI supports many MIPS-based evaluation boards which can be accessed through a variety of interfaces:

- **Bare Board Access (no RTOS or ROM Monitor)**—MULTI supports on-chip debugging through JTAG (EJTAG) hardware through the MDI (MIPS Debug Interface) protocol. MIPS-based boards from MIPS Technologies, IDT, NEC, Philips, Toshiba, Broadcom, Intrinsity, LSI Logic and others are supported by the Green Hills Probe™ and Slingshot™, EPI MAJIC™, Macraigor OCD, Agilent Emulation Probe and First Silicon Solutions probe.
- **ROM Monitors**—MULTI supports a variety of boards with PMON and IDTsim.
- **Commercial RTOS Support**—MULTI supports MIPS boards running Green Hills Software's royalty-free *velOSity* microkernel and INTEGRITY RTOS, ThreadX from Express Logic, and Tornado/VxWorks from Wind River Systems. MULTI provides multitask-aware debugging, and special commands that allow tasks to be stopped upon system events such as task creation.
- **Run-Mode Debugging**—Run-Mode enables source debugging of one or more threads of execution within their own colored debug window, allowing the rest of the system to continue to run, handling real-time events. This advanced feature adds very little overhead to the embedded program making it ideal for deeply embedded real-time applications.
- **Custom RTOS Support**—MULTI can be interfaced with a custom RTOS through integration of the Green Hills INDRT API.
- **Instruction Set Simulators (ISS)**—MULTI is tightly integrated with Instruction Set Simulators to provide complete debug capabilities that would be available with a hardware target: host I/O, command windows, extended profiling and hardware breakpoints. This enables users to prototype embedded applications early in the development cycle when silicon is unavailable. The Simmips ISS simulates the execution of the target processor at the instruction level. The MIPSsim ISS from MIPS Technologies is available as an Instruction Accurate or Cycle Accurate model. Both Simmips and MIPSsim simulate target CPU cache for those processors which support it.

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